REMARKS

The Applicant does not believe that examination of the foregoing amendment will result in the introduction of new matter into the present application for invention. Therefore, the Applicant, respectfully, requests that the above amendment be entered in and that the claims to the present application, kindly, be reconsidered.

The Office Action dated November 3, 2006 has been received and considered by the Applicant. The November 3, 2006 Office Action states that Claims 1-7 are pending in the present application; this is incorrect. The previous response by the Applicant added Claim 8-20. Therefore, Claims 1-20 are pending in the present applicant for invention. There are no rejections to Claims 8-20 contained within the November 3, 2006 Office Action.

Claims 1-7 are rejected by the November 3, 2006 Office Action Office Action.

Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,502,512 issued in the name of Toyoda et al. (hereinafter referred to as Toyoda et al.) in view of US Patent No 5,923,892 issued in the names of Levy (hereinafter referred to as Levy).

The MPEP at §2143 states that to "establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.

The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)."

Regarding Claim 1, the rejection asserts that Toyoda et al. disclose an apparatus and method for digital video and audio processing with information input and output processing devices. The rejection reads the subject matter for a "first domain processing means for first processing data depending on first domain configuration information" extremely broadly and asserts that this subject matter is taught by Toyoda et

al. The Applicant, respectfully, points out that Col 2, lines 49-52 as well as numerals 101, 102, and 103 in FIG. 1 of Toyoda et al, teach information processing means 101, 102 and 103 are for entering video or audio information, and putting out directly or after arithmetic processing of video or audio information. The Applicant, respectfully, asserts that Toyoda et al. do not disclose, or suggest, first domain processing means for first processing data depending on first domain configuration information. There is no dependency disclosed on first domain configuration information disclosed or suggested by Toyoda et al.

The Applicant further asserts that Toyoda et al. do not disclose, or suggest, each first domain processor differently sub-processing the data in order to first process the data.

The Examiner states item 102 in Fig. 1 teaches the subject matter for a "second domain processing means (110) for second processing the first processed data depending second domain configuration information, the second processing being different than the first processing". The Applicant does not concur with this assertion. Toyoda et al. at Col 4, lines 31-34 the state that the "operations of the information input and output processing means 101, 102 and 103 are controlled by the control means 105 in which the control information is entered from the input means 106." The foregoing does not disclose or suggest the subject matter for the second domain processing means second processing the first processed data depending on the configuration of the second domain information with the second processing being different than the first processing.

The Applicant further asserts that Toyoda et al. do not disclose, or suggest, each second domain processor differently sub-processing the data in order to second process the data.

The Applicant further asserts that rejected Claim 1 defines subject matter for a first domain control processor and a second domain control processor; which are not addressed by the Office Action. Therefore, all the features within the rejected claims are not found in the combination made by the Office Action and a *prima facie* case of obviousness is not made.

The Examiner further states that the subject matter of "a global control processor (120) connected to the communication means for providing the first domain

configuration information and the second domain configuration information through the configuring first and second domains" is met by Control means 105. The Applicant does not concur with this assertion. The Examiner's position is that Toyoda et al. at Col 4, lines 31-34 disclose that the process to be executed by the "domains' is controlled by the control means 105. The Applicant does not concur with this assertion. Toyoda et al. at Col 4, lines 31-34 the state that the "operations of the information input and output processing means 101, 102 and 103 are controlled by the control means 105 in which the control information is entered from the input means 106." Toyoda et al. do not disclose, or suggest, a global control processor (120) connected to the communication means for providing the first domain configuration information and the second domain configuration information through the configuring first and second domains.

The rejection admits that Toyoda et al. fail to disclose the concept the first and second "domains" having multiple processors as defined by the rejected claims. The rejection contends that Levy teaches using multiple processors in a particular "domain' so as to improve the overall speed and efficiency. The Applicant asserts that Levy does not disclose, or suggest, the subject matter for each first domain processor differently sub-processing the data in order to first process the data. The Applicant further asserts that Levy does not disclose, or suggest, the subject matter for each second domain processor differently sub-processing the data in order to second process the data.

The Applicant, respectfully, points out that rejected Claim 1 defines subject matter for the first domain processors including a first domain control processor for controlling the first processing of the first domain and the second domain processors including a second domain control processor for controlling the second processing of the second domain. It should be noted that there is no mention of the first domain control processor or the second domain control processor within the rejection. Therefore, all the subject matter defined by rejected Claim 1 is not found in the combination made by the rejection.

The Applicant, respectfully, points out that rejected Claim 1 defines subject matter for each first domain processor differently sub-processing the data in order to first process the data and for each second domain processor differently sub-processing the data in order to second process the data. It should be noted that the Office Action

does not address the subject matter for each first domain processor differently sub-processing the data in order to first process or each second domain processor differently sub-processing the data in order to second process the data within the rejection. Therefore, all the subject matter defined by rejected Claim 1 is not found in the combination made by the rejection.

For the foregoing reasons, this rejection is, respectfully, traversed.

Claims 2 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Toyoda et al. in view Levy, further in view of U.S. Patent Publication No. 2003/0032390 is the names of Geile et al. (hereinafter referred to as Geile et al.) and further in view of US Patent No 5,844,941 issued in the names of Macket et al. (hereinafter referred to as Macket et al.).

Regarding claims 2 and 7, the rejection asserts that claimed limitations of "the communication means include a stream-based communication means connected to the global control processor and connected to a plurality of the processors of the first and second domains including the first and second domain control processors for transmitting information streams between connected processors" and "the stream-based communications means are connected to an input/output bus to at times receive stream of data into the multi-processor unit through the stream-based communications means in to one of the connected processors and to at other times transmit a stream of data from one of the connected processors through the stream-based communications means onto the input/output bus" are met by the bus means 107 within Figure 1 of Toyoda et al. The Applicant does not concur with this assertion. Toyoda et al. do not disclose, or suggest, the subject matter for the communication means include a stream-based communication means connected to the global control processor and connected to a plurality of the processors of the first and second domains including the first and second domain control processors for transmitting information streams between connected processors.

The Examiner admits that the combination fails to disclose blocks of memory with selective interconnections to the plurality of processors. The rejection alleges that Levy teaches block of memory with selective interconnection to a plurality of

processors at col. 7, line 61-col. 8, line 20. The Applicant disagrees. Levy simply discuses that memory transfers that are handled via DMA. There is no disclosure or suggestion for blocks of memory with selective interconnections to the plurality of processors within Levy.

The Applicant respectfully points out that Claims 2 and 7 define subject matter for a multi-processor unit that includes blocks of electronic memory, the communication means includes block-based communication means connected to the processors and a processors for selectively interconnecting the connected processors to the memory blocks, with only one processor at a time being interconnected to one of the memory blocks, and processors of different domains being interconnected at different times to the same memory block. This subject matter is not disclosed or suggested by the cited prior art references.

The rejection admits that the combined teaching of Toyoda et al. with Levy fails to disclose that Geile et al. the processing includes FFT and IFFT processing. The Examiner alleges that Geile et al. teaches FFT and IFFT processing. The Applicant points out that Claim 2 defines that the processing of the first domain includes FFT and IFFT. There is no disclosure or suggestion that the processing of the first domain within a multi-domain multi-processing unit includes FFT and IFFT within Geile et al.

The rejection admits that the combined teaching of Toyoda et al. with Levy fails to disclose the use of a periodic sequencer. The rejection alleges that Geile et al. teache periodic processing. The Applicant points out that Claim 2 defines that "at least one of the domain processors includes a periodic sequencer". This subject matter is not disclosed or suggested by the combination of Toyoda et al. with Levy, Geile et al. and Macket et al. The rejection only finds a sequencer; which alone does not address the foregoing subject matter.

The Applicant, respectfully points out that Claim 2 defines subject matter for at least one of the domain control processors includes a periodic sequencer that initiates control commands transmitted to other processors to initiate subroutines in those processors depending on an index counter. The rejection alleges that the combination of Toyoda et al. with Levy, Geile et al. and Macket et al. teaches a periodic sequencer.

Specifically, the Examiner states that Macket et al. at col. 8, line 60-col. 9, line 28 teach equalization of a stored received signal for reconstruction. The Applicant assert that this allegation does not reach the subject matter for at least one of the domain control processors includes a periodic sequencer that initiates control commands transmitted to other processors to initiate subroutines in those processors depending on an index counter.

In view of the aforesaid reasons and arguments, this rejection is traversed.

Claims 3-6 are rejected under 35 U. S. C. 103(a) as being unpatentable over Toyoda et al, with Levy and further in view of Integrated Circuits and Microprocessors by R.C. Holland. Claims 3-6 depend from claims that have been previously discussed and are believed to be allowable and further narrow and define these claims. Therefore, Claims 3-6 are also believed to be allowable.

Claim 8-20 have not been addressed by the Office Action. Therefore, there are no rejections to Claims 8-20; which are believed to be allowable.

Applicant is not aware of any additional patents, publications, or other information not previously submitted to the Patent and Trademark Office which would be required under 37 C.F.R. 1.99.

In view of the foregoing amendment and remarks, the Applicant believes that the present application is in condition for allowance, with such allowance being, respectfully, requested.

Please charge any fees, except for the issue fee, to Account No. 50-3745, and credit any funds to that same account.

Respectfully submitted,

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